IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application No.: 10/821,729	§	Examiner:	Verderamo III, R
Filed: April 9, 2004	§	Group/Art Unit:	2186
Inventor(s):	§	Atty. Dkt. No:	5681-13301
Landin et al.	§	Confirm No.	1516
	§		
	§		
Title: Multi-Node Computer System Where Active Devices Selectively Initiate Certain Transactions Using Remote-Type Address Packets	§		

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir/Madam:

Further to the Notice of Appeal of March 17, 2008, Appellant presents this Appeal Brief. Appellant respectfully requests that this appeal be considered by the Board of Patent Appeals and Interferences.

I. REAL PARTY IN INTEREST

The subject application is owned by Sun Microsystems Inc. An assignment of the present application to the owner is recorded at Reel 015843, Frame 0558.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences known to Appellant.

III. STATUS OF CLAIMS

Claims 1-42 are pending. Claims 1-9, 12-23, 26-36, and 39-42 are rejected under 35 U.S.C. § 102(b). Claims 10, 11, 24, 25, 37 and 38 are rejected under 35 U.S.C. § 103(a). It is these rejections that are being appealed. A copy of claims 1-42 is included in the Claims Appendix attached hereto.

IV. STATUS OF AMENDMEMNTS

No unentered amendment to the claims has been filed after final rejection. The Appendix hereto reflects the current state of the rejected claims.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

Independent claim 1 is directed to a system (*See*, e.g., Fig. 20, #100) that includes an inter-node network (*See*, e.g., Fig. 20, #154) and a plurality of nodes (*See*, e.g., Fig. 20, #140A, #140B, and #140C) coupled by the inter-node network. Each of the plurality of nodes includes a plurality of active devices (*See*, e.g., Fig. 20, #142AA, #142BA, #146A, #142AB, #142BB, 146B, #142AC, #142BC, 146C; and specification page 11, lines 16-18), an interface (*See*, e.g., Fig. 20, #148A, #148B, #148C) configured to send and receive coherency messages on the inter-node network (*See*, e.g., specification page 63, lines 7-10), and an address network (*See*, e.g., Fig. 20, #150A, #150B, 150C) coupling the plurality of active devices to the interface. In addition, an active device (*See*, e.g., Fig. 20, #142AA) included in a node of the plurality of nodes is configured to initiate a write back transaction involving a coherency unit by sending either a first type of address packet or a second type of address packet on the address network dependent on whether the active device is included in a multi-node system (*See*, e.g., specification page 122, line 19 - page 123, line 6).

Independent claim 16 is directed to a node (*See*, e.g., Fig. 20, #140A, #140B, and #140C) that includes a plurality of devices (*See*, e.g., Fig. 20, #142AA, #142BA, #146A, #148A) coupled by an address network (*See*, e.g., Fig. 20, #150A), wherein the plurality of devices includes an active device (*See*, e.g., Fig. 20, #142AA) and an interface (*See*, e.g., Fig. 20, #148A) configured to communicate via an inter-node network (*See*, e.g., Fig. 20, #154, specification page 63, lines 7-10) coupling nodes in a multi-node system. The active device (*See*, e.g., Fig. 20, #142AA) is configured to initiate a write back transaction involving a coherency unit by sending either a first type of address packet or a second type of address packet on the address network dependent on whether the active device is included in a multi-node system or a single node system (*See*, e.g., specification page 122, line 19 - page 123, line 6).

Independent claim 28 is directed to a method of operating a multi-node system (*See*, e.g., Fig. 20, #100) that includes a plurality of nodes (*See*, e.g., Fig. 20, #140A,

#140B, and #140C) coupled by an inter-node network (*See*, e.g., Fig. 20, #154). Each of the plurality of nodes includes a plurality of active devices (*See*, e.g., Fig. 20, #142AA, #142BA, #146A, #142AB, #142BB, 146B, #142AC, #142BC, 146C; and specification page 11, lines 16-18), an interface (*See*, e.g., Fig. 20, #148A, #148B, #148C) configured to send and receive coherency messages on the inter-node network (*See*, e.g., specification page 63, lines 7-10), and an address network (*See*, e.g., Fig. 20, #150A, #150B, 150C) coupling the plurality of active devices to the interface. The method includes an active device (*See*, e.g., Fig. 20, #142AA) included in a node of the plurality of nodes detecting whether the active device is included in a multi-node system (*See*, e.g., specification page 123, lines 17-19). The method also includes an active device included in a node of the plurality of nodes initiating a write back transaction involving a coherency unit by sending either a first type of address packet or a second type of address packet on an address network included in the node dependent on said detecting (*See*, e.g., specification page 122, line 19 - page 123, line 6).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Claims 1-9, 12-23, 26-36, and 39-42 are rejected under 35 U.S.C. § 102(b) as being unpatentable over Hunter et al. (U.S. Patent No. 5,394,555).

2. Claims 10, 24, and 37 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Hunter in view of Farmwald et al. (U.S. Patent No. 5,606,717).

3. Claims 11, 25, and 38 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Hunter in view of Baxter et al. (U.S. Patent No. 5,887,146), and in further view of Martin et al. ("Bandwidth Adaptive Snooping") (hereinafter "Martin").

VII. ARGUMENT

First Ground of Rejection:

Claims 1-9, 12-23, 26-36, and 39-42 are rejected under 35 U.S.C. § 102(a) as being unpatentable over Hunter. Appellant traverses this rejection for at least the following reasons.

Independent claims (by number):

Appellant respectfully submits that each of claims 1, 16, and 28 recites features not taught or disclosed in Hunter. For example, claim 1 recites a system comprising in pertinent part

> a plurality of nodes coupled by the inter-node network, wherein each of the plurality of nodes includes a plurality of active devices, an interface configured to send and receive coherency messages on the inter-node network, and an address network coupling the plurality of active devices to the interface;
> wherein **an active device** included in a node of the plurality of nodes is configured to **initiate a write back transaction** involving a coherency unit **by sending either a first type of address packet or a second type of address packet** on the address network **dependent on whether the active device is included in a multi-node system**. (Emphasis added)

In the final Office action dated December 18, 2007, the Examiner asserts Hunter teaches each and every limitation recited in Appellant's claim 1. Appellant respectfully disagrees with the Examiner's characterization of Hunter and the application of Hunter to Appellant's claims. More particularly, the Examiner asserts Hunter teaches the limitations at col. 4, lines 20-25. Appellant disagrees. Specifically, Hunter actually discloses

> The DSBA is an environment which offers the simplest way to understand the real-time operation of SOs. Referring to FIG. 2, each node in the cluster (only two nodes of two CPUs 1 each are shown for simplicity) contains an **External Coherency Unit (ECU)** 10 that: (a) **snoops its own node-local bus 4 for commands on shared cache-lines that are also present in other nodes**, and (b) **conditionally forwards these commands (using a unique identifier for the cache-line) to the other nodes via, for**

> **example, a separate inter-node ECU bus** 11. (Point-to-point connections are also possible, using a directory in each ECU to keep track of which nodes have copies.) All other **ECUs**: (a) snoop the inter-node ECU bus 11 for commands that affect cache-lines resident in their own local memories, (b) translate these to their own physical tags and (c) inject the translated commands into their own node-local buses. (*See* col. 4, lines 9-25) (Emphasis added)

From the foregoing disclosure, it is clear to Appellant that Hunter is disclosing the CPU (the active device not the ECU) sending **one type of command** within the node, and the **ECU (interface) within the same node** sends the command with a unique identifier across the ECU bus. An ECU within a different node translates the command into physical tags and then sends the translated commands within the other node based upon snooping traffic on the various internal and external buses. Furthermore the ECU sends the different command dependent upon whether the cache line is present in another node, not whether there is another node present. This is clearly not the same as **a given active device (e.g., CPU) within in a node** sending on an internal bus within the node one type of address packet (command) if it is in a multinode system, and a different type of address packet if it is not in a multinode system.

The Examiner further asserts in the Advisory action dated March 18, 2008, "the ECU can also be interpreted as an active device of the node (which is what is required by claim 1). Once a command is placed on the bus a ECU will either retrieve the data directly from local memory (first type of command) or if the state is invalid or shared remote action is taken (second type of command) (column 6, lines 21-45. Examiner also refers to column 6, lines 12-20. ECU determines if inter-node action is required. If the system were not in a multi-node system it would determine that inter-node action is not required." Appellant respectfully submits that even though the ECU may be considered as an active device as the Examiner is suggesting, the ECU still does not fulfill the requirements of claim 1. Appellant submits the Examiner's characterization is faulty. Specifically, Hunter discloses

> Referring again to FIG. 3, the ECU 10 ignores commands for non-shared cache-line requests which proceed directly to address the

> identified memory in the non-shared physical space 14 of the local memory 3. However, when the ECU identifies a command for a shared cache-line, it examines its coherence state (modified, exclusive, shared, or invalid), which is stored in the ECU directory 16, to determine if any inter-node action is required to maintain coherence. If inter-node action is required, the physical address is translated to the appropriate unique identifier and transmitted, together with the appropriate command **over the ECU bus** to other nodes in the cluster.
> For example, if a CPU wishes to obtain an exclusive copy of a shared cache-line, it places a suitable command (e.g., RTW--"read with intent to write"--in the exemplary system to be explained more fully below) on its node-local bus which will cause each ECU 10 to take the following set of possible actions:
> (1) if the cache-line state is exclusive or modified, it will be retrieved directly from local memory 3 and sent to the requesting processor with no remote action taken because no other copies exist;
> (2) if the state is invalid, an RTW command will be transmitted over the inter-node ECU bus 11 to other nodes. A remote node that contains the line in exclusive or modified state will transmit (siphon) the cache line over the inter-node ECU bus to the requester. If several nodes contain the line in the shared state, all attempt to send it, but ECU bus conventional priority logic will choose one and cancel the others. All remote copies will be set to the invalid state.
> (3) if the state is shared, the INV command will be sent to other nodes, which cause them to set their states to invalid (siphoning is not necessary because a current copy already exists in the requesting node). (*See* col. 6, lines 8-45) (Emphasis added)

From the foregoing passages, and in contrast to the Examiner's assertions, Appellant submits in the Examiner's example, the RTW command initiated by a requesting CPU causes data to be retrieved from local memory via the node local bus 4 (and without additional ECU intervention), and if remote action is required, the ECU sends an RTW command on the internode ECU (external to the node) bus 11. Thus, the ECU sends the command on an external bus to other nodes.

Accordingly, Appellant submits Hunter does not teach or disclose "wherein an active device included in a node of the plurality of nodes is configured to initiate a write

back transaction involving a coherency unit by sending either a first type of address packet or a second type of address packet **on the address network** dependent on whether the active device is included in a multi-node system," as recited in claim 1.

Claims 16 and 28, recite features that are similar to the features recited in claim 1, and are believed to patentably distinguish over Hunter for the reasons given above in regard to claim 1.

For at least the above stated reasons, Appellant submits that the rejection of claims 1, 16, and 28 is in error and requests reversal of the rejection. The rejection of claims 2-15 (dependent from claim 1), claims 17-27 (dependent from claim 16), and claims 29-42 (dependent from claim 28) is similarly in error for at least the above stated reasons, and reversal of the rejection is requested. Each of claims 1-15, 17-27, and 29-42, recite additional features not taught or suggested in the cited art.

Second Ground of Rejection:

Claims 10, 24, and 37 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Hunter in view of Farmwald. Appellant traverses this rejection for at least the following reasons.

In addition to the reasons given above in regard to claim 1, Appellant respectfully submits claim 10 further distinguishes over the cited art for the following reasons.

The Examiner asserts Hunter teaches the owner of a node providing data about a coherency unit at col. 6, lines 31-40, and acknowledges Hunter does not teach the use of a NACK packet. The Examiner further asserts Farmwald teaches the use of a NACK packet. Appellant respectfully disagrees with the Examiner's characterization of Hunter and the combination of Hunter and Farmwald. More particularly, Appellant submits the claim recites far more language than just the use of a NACK. Specifically, as shown above, in col. 6, lines 21-40 Hunter is merely teaching a CPU requesting a cache line

locally, and if the cache line state is exclusive, the cache line is retrieved locally, if the state is invalid, the RTW command is sent by an ECU in the node to other nodes. Another node that owns the line retrieves the data and provides it to the requester. If several nodes have the cache line in the shared state, they may all try to send it but the ECU will choose one and cancel the others.

Farmwald is directed to a memory circuit and merely discloses the use of NACK signaling.

Appellant fails to see how the above disclosure in Hunter and Farmwald teaches "… **if the active device sends the RWB** address packet **and another active device included in the node gains ownership** of the coherency unit **before** an interface included in the node sends a responsive address packet, the other active device is configured to provide data to the interface in response to the responsive address packet;" or "wherein **if** the active device **sends the WB** address packet and **the other active device included in the node gains ownership** of the coherency unit **before a memory subsystem included in the node sends a different responsive address packet**, the active device is configured to send a **NACK data packet** to the memory subsystem," as recited in claim 10. Appellant contends it does not.

Accordingly, Appellant submits that the rejection of claims 1, 16, and 28 is in error and requests reversal of the rejection.

Third Ground of Rejection:

Claims 11, 25, and 38 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Hunter in view of Baxter. Appellant traverses this rejection for at least the reasons given above in regard to the discussion of claim 1.

CONCLUSION

For the foregoing reasons, it is submitted that the Examiner's rejection of claims 1-42 is erroneous, and reversal of his decision is respectfully requested.

The Commissioner is authorized to charge any fees that may be due to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5681-13301/SJC.

Respectfully submitted,

/ Stephen J. Curran /
Stephen J. Curran
Reg. No. 50,664
AGENT FOR APPELLANT(S)

Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C.
P.O. Box 398
Austin, TX 78767-0398
Phone: (512) 853-8800

Date: May 19, 2008

VIII. APPENDIX

The claims on appeal are as follows.

1. A system, comprising:

an inter-node network; and

a plurality of nodes coupled by the inter-node network, wherein each of the plurality of nodes includes a plurality of active devices, an interface configured to send and receive coherency messages on the inter-node network, and an address network coupling the plurality of active devices to the interface;

wherein an active device included in a node of the plurality of nodes is configured to initiate a write back transaction involving a coherency unit by sending either a first type of address packet or a second type of address packet on the address network dependent on whether the active device is included in a multi-node system.

2. The system of claim 1, wherein the first type of address packet is a remote write back (RWB) address packet and the second type of address packet is a write back (WB) address packet, wherein the active device is configured to send the RWB address packet if the active device is included in a multi-node system, and wherein each active device included in the node having access to or ownership of the coherency unit is configured to ignore the RWB address packet;

wherein each active device included in the node having access to or ownership of the coherency unit is configured to transition an access right to or an ownership responsibility for the coherency unit in response to the second type of address packet.

3. The system of claim 2, wherein the active device is configured to send the RWB address packet if the active device is included in a multi-node system and if the coherency unit is not mapped by any memory subsystem included in the node.

4. The system of claim 3, wherein an interface included in the node is configured to send a coherency message via the inter-node network to a home node for the coherency unit in response to receiving the remote write back address packet, and wherein each active device included in the node is configured to ignore the remote write back address packet.

5. The system of claim 4, wherein a home interface in the home node is configured to lock the coherency unit in response to the coherency message and to responsively send an additional coherency message requesting initiation of a proxy read-to-own-modified subtransaction to the interface in the node.

6. The system of claim 5, wherein in response to receiving the additional coherency message, the interface in the node is configured to send a proxy read-to-own-modified address packet on the address network.

7. The system of claim 6, wherein each active device included in the node having an access right to the coherency unit and not having an ownership responsibility for the coherency unit is configured to invalidate the access right in response to the proxy read-to-own modified address packet.

8. The system of claim 6, wherein the active device is configured to transition an ownership responsibility for the coherency unit upon receipt of the proxy read-to-own modified address packet and to responsively send a data packet corresponding to the coherency unit to the interface.

9. The system of claim 8, wherein the active device is configured to transition an access right corresponding to the coherency unit upon sending the data packet.

10. The system of claim 2, wherein the active device is configured to send the RWB address packet if the active device is included in a multi-node system and the WB address packet if the active device is included in a single node system;

wherein if the active device sends the RWB address packet and another active device included in the node gains ownership of the coherency unit before an interface included in the node sends a responsive address packet, the other active device is configured to provide data to the interface in response to the responsive address packet;

wherein if the active device sends the WB address packet and the other active device included in the node gains ownership of the coherency unit before a memory subsystem included in the node sends a different responsive address packet, the active device is configured to send a NACK data packet to the memory subsystem.

11. The system of claim 1, wherein the active device includes a mode register configured to store a value indicating whether the active device is included in a multi-node system.

12. The system of claim 1, wherein the first type of address packet is a remote write stream address packet (RWS) and the second type of address packet is a write stream address packet (WS), wherein the active device is configured to send the (RWS) address packet if the active device is included in a multi-node system and to send the WS address packet if the active device is included in a single node system.

13. The system of claim 12, wherein an interface included in the node is configured to respond to the first type of address packet by sending a coherency message via the inter-node network to a home node for the coherency unit, and wherein active devices and memory subsystems included in the node are configured to ignore the first type of address packet.

14. The system of claim 13, wherein in response to the coherency message, a home interface included in the home node is configured to lock the coherency unit and to

responsively send an invalidating coherency message to one or more ones of the plurality of nodes and to send a write stream coherency message to the interface in the node.

15. The system of claim 14, wherein the interface in the node is configured to send a pull request data packet to the active device in response to receiving acknowledgment coherency messages from each of the one or more ones of the plurality of nodes that received the invalidating coherency message;

wherein in response to the pull request data packet, the active device is configured to send an additional data packet containing a copy of the coherency unit to the interface.

16. A node, comprising:

a plurality of devices coupled by an address network, wherein the plurality of devices includes an active device and an interface configured to communicate via an inter-node network coupling nodes in a multi-node system;

wherein the active device is configured to initiate a write back transaction involving a coherency unit by sending either a first type of address packet or a second type of address packet on the address network dependent on whether the active device is included in a multi-node system or a single node system.

17. The node of claim 16, wherein the first type of address packet is a remote write back address (RWB) packet and the second type of address packet is a write back (WB) address packet, wherein the active device is configured to send the first type of address packet if the active device is included in a multi-node system, and wherein each active device included in the node having access to or ownership of the coherency unit is configured to ignore the RWB address packet;

wherein each active device included in the node having access to or ownership of the coherency unit is configured to transition an access right to or an ownership responsibility for the coherency unit in response to the WB address packet.

18. The node of claim 17, wherein the active device is configured to send the remote write back address packet if the active device is included in a multi-node system and if the coherency unit is not mapped by any memory subsystem included in the node.

19. The node of claim 18, wherein the interface is configured to send a coherency message via the inter-node network to a home node for the coherency unit in response to receiving the remote write back address packet, and wherein each active device included in the node is configured to ignore the remote write back address packet.

20. The node of claim 19, wherein in response to receiving a responsive coherency message from the home node for the coherency unit, the interface in the node is configured to send a proxy read-to-own-modified address packet on the address network.

21. The node of claim 20, wherein each active device included in the node having an access right to the coherency unit and not having an ownership responsibility for the coherency unit is configured to invalidate the access right in response to the proxy read-to-own modified address packet.

22. The node of claim 20, wherein the active device is configured to transition an ownership responsibility for the coherency unit upon receipt of the proxy read-to-own modified address packet and to responsively send a data packet corresponding to the coherency unit to the interface.

23. The node of claim 22, wherein the active device is configured to transition an access right corresponding to the coherency unit upon sending the data packet.

24. The node of claim 17, wherein the active device is configured to send the RWB address packet if the active device is included in a multi-node system and the WB address packet if the active device is included in a single node system;

wherein if the active device sends the RWB address packet and another active device included in the node gains ownership of the coherency unit before the interface sends a responsive address packet, the other active device is configured to provide data to the interface in response to the responsive address packet;

wherein if the active device sends the WB address packet and the other active device included in the node gains ownership of the coherency unit before a memory subsystem included in the node sends a different responsive address packet, the active device is configured to send a NACK data packet to the memory subsystem.

25. The node of claim 16, wherein the active device includes a mode register configured to store a value indicating whether the active device is included in a multi-node system.

26. The node of claim 16, wherein the first type of address packet is a remote write stream (RWS) address packet and the second type of address packet is a write stream (WS) address packet, wherein the active device is configured to send the RWS address packet if the active device is included in a multi-node system and to send the WS address packet if the active device is included in a single node system.

27. The node of claim 26, wherein the interface is configured to respond to the RWS address packet by sending a coherency message via the inter-node network to a home node for the coherency unit, and wherein active devices and memory subsystems included in the node are configured to ignore the RWS address packet.

28. A method of operating a multi-node system comprising a plurality of nodes coupled by an inter-node network, wherein each of the plurality of nodes includes a

plurality of active devices, an interface configured to send and receive coherency messages on the inter-node network, and an address network coupling the plurality of active devices to the interface, the method comprising:

an active device included in a node of the plurality of nodes detecting whether the active device is included in a multi-node system; and

an active device included in a node of the plurality of nodes initiating a write back transaction involving a coherency unit by sending either a first type of address packet or a second type of address packet on an address network included in the node dependent on said detecting.

29. The method of claim 28, wherein the first type of address packet is a remote write back (RWB) address packet and the second type of address packet is a write back (WB) address packet, and wherein the active device sends the RWB address packet if the active device is included in a multi-node system, the method further comprising:

each active device included in the node having access to or ownership of the coherency unit ignoring the RWB address packet; and

each active device included in the node having access to or ownership of the coherency unit transitioning an access right to or an ownership responsibility for the coherency unit in response to the WB address packet.

30. The method of claim 29, further comprising:

the active device sending the RWB address packet if the active device is included in a multi-node system and if the coherency unit is not mapped by any memory subsystem included in the node.

31. The method of claim 30, further comprising:

an interface included in the node sending a coherency message via the inter-node network to a home node for the coherency unit in response to receiving the remote write back address packet; and

each active device included in the node ignoring the remote write back address packet.

32. The method of claim 31, further comprising a home interface in the home node locking the coherency unit in response to the coherency message and responsively sending an additional coherency message requesting initiation of a proxy read-to-own-modified subtransaction to the interface in the node.

33. The method of claim 32, further comprising the interface in the node sending a proxy read-to-own-modified address packet on the address network in response to receiving the additional coherency message.

34. The method of claim 33, further comprising each active device included in the node having an access right to the coherency unit and not having an ownership

responsibility for the coherency unit invalidating the access right in response to the proxy read-to-own modified address packet.

35. The method of claim 33, further comprising the active device transitioning an ownership responsibility for the coherency unit upon receipt of the proxy read-to-own modified address packet and responsively sending a data packet corresponding to the coherency unit to the interface.

36. The method of claim 35, further comprising the active device transitioning an access right corresponding to the coherency unit upon sending the data packet.

37. The method of claim 29, further comprising:

the active device sending the RWB address packet if the active device is included in a multi-node system and the WB address packet if the active device is included in a single node system;

if the active device sends the RWB address packet and another active device included in the node gains ownership of the coherency unit before an interface included in the node sends a responsive address packet, the other active device providing data to the interface in response to the responsive address packet;

if the active device sends the WB address packet and the other active device included in the node gains ownership of the coherency unit before a memory subsystem included in the node sends a different responsive

address packet, the active device sending a NACK data packet to the memory subsystem.

38. The method of claim 28, further comprising a mode register included in the active device storing a value indicating whether the active device is included in a multi-node system.

39. The method of claim 28, wherein the first type of address packet is a remote write stream (RWS) address packet and the second type of address packet is a write stream (WS) address packet, the method further comprising:

the active device sending the RWS address packet if the active device is included in a multi-node system and sending the WS address packet if the active device is included in a single node system.

40. The method of claim 39, further comprising:

an interface included in the node responding to the RWS address packet by sending a coherency message via the inter-node network to a home node for the coherency unit, wherein active devices and memory subsystems included in the node ignore the RWS address packet.

41. The method of claim 40, further comprising:

in response to the coherency message, a home interface included in the home node locking the coherency unit and responsively sending an invalidating coherency message to one or more ones of the plurality of nodes and sending a write stream coherency message to the interface in the node.

42. The method of claim 41, further comprising:

the interface in the node sending a pull request data packet to the active device in response to receiving acknowledgment coherency messages from each of the one or more ones of the plurality of nodes that received the invalidating coherency message;

in response to the pull request data packet, the active device sending an additional data packet containing a copy of the coherency unit to the interface.

IX. EVIDENCE APPENDIX

No evidence submitted under 37 C.F.R. §§ 1.130, 1.131, or 1.132 or otherwise entered by the Examiner is relied upon in this appeal.

X. RELATED PROCEEDINGS APPENDIX

There are no related proceedings.